What is claimed is:

1. A method for debugging, comprising steps of:

sending a system management interrupt signal to trigger a debugging tool program;

executing each debugging item in said debugging tool program; and

returning to current operation system after debugged.

2. The method of claim 1, wherein said debugging tool program is provided in a system management mode of BIOS.

3. The method of claim 1, wherein said debugging item comprises access input and output, access memory, access device configuration and trap set for specific IO address.

4. The method of claim 1, wherein said step of executing each debugging item in said debugging tool program could be operated in a debugging operation window.

5. The method of claim 4, wherein said debugging operation window is programmable.

6. A method for debugging, implemented in a computer system, including a central processing unit connected to a chipset, said method comprising:

Sending a system management interrupt signal from said chipset to said central processing unit;

executing to pop out a debugging operation window after said central processing unit staid in a system management mode;

selecting and executing each debugging item; and

Leaving the debugging operation window after end of execution ;

Wherein finished the debugging execution, said central process unit is able to execute next queued instruction.

7. The method of claim 6, wherein said debugging item comprises access input and output, access memory, access device configuration and trap set for specific IO address.

8. The method of claim 6, wherein said debugging operation window is programmable.

9. The method of claim 6, wherein before the step of said chipset sending said system management interrupt signal to said central processing unit, said chipset is triggered by users through a predetermined general purpose input/output pin.

10. The method of claim 6, further comprising a step of after leaving said debugging operation window after end of execution, said debugging operation window would be popped out next time when said chipset triggered by users again.

11. The method of claim 6, further comprising a step of after leaving said debugging operation window after end of execution, said debugging operation window would be popped out from a predetermined trap address.

12. A device for debugging, which comprises:

a central processing unit; and

a chipset connected to said central processing unit, including a system management interrupt pin for sending system management interrupt signal, and a plurality of general purpose input/output pins for being used to trigger by users.

13. The device of claim 12, wherein said central processing unit is connected with at lease one memory.

14. The device of claim 13, wherein said memory comprises a system management mode section.

15. The device of claim 14, wherein said system management mode section comprises a debugging tool program.

16. The device of claim 15, wherein said debugging tool program comprises a popping out debugging operation window.

17. The device of claim 12, wherein said system management interrupt signal is sent through said system management interrupt pin when said chipset triggered by users.

18. The device of claim 12, wherein said system management interrupt signal is sent through the links between chipsets and central processing unit when said chipset triggered by users

19. The device of claim 17, wherein said system management interrupt signal enables said central processing unit to move into said system management mode section to execute said debugging tool program.

20. The device of claim 17, wherein said chipset is presented as a south-bridge chipset.